

FIG.1 (a)

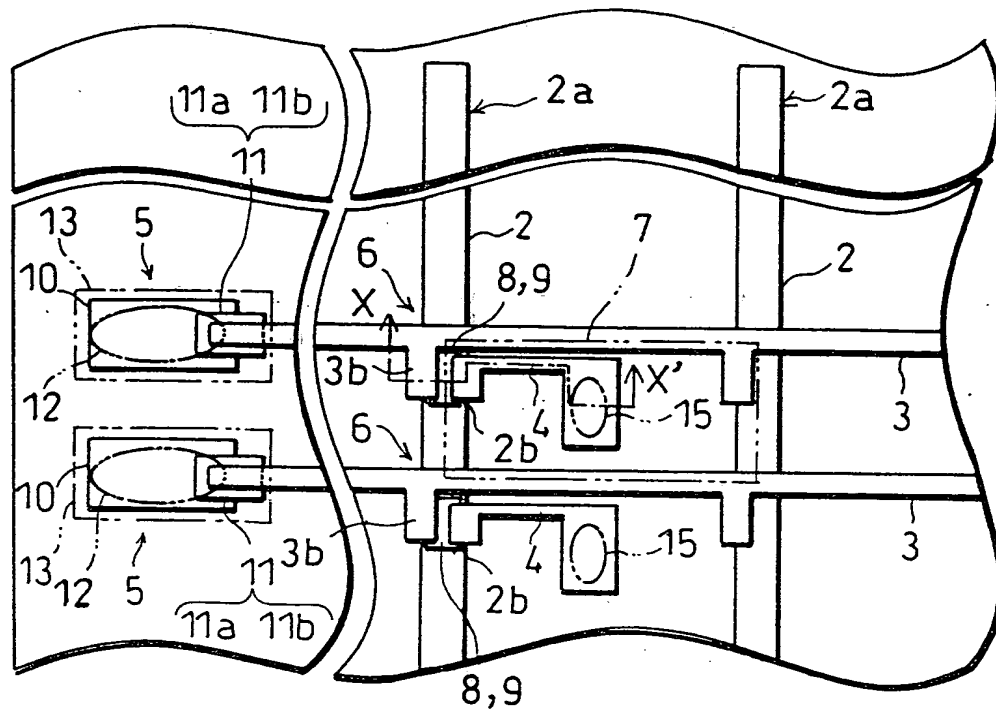


FIG.1 (b)

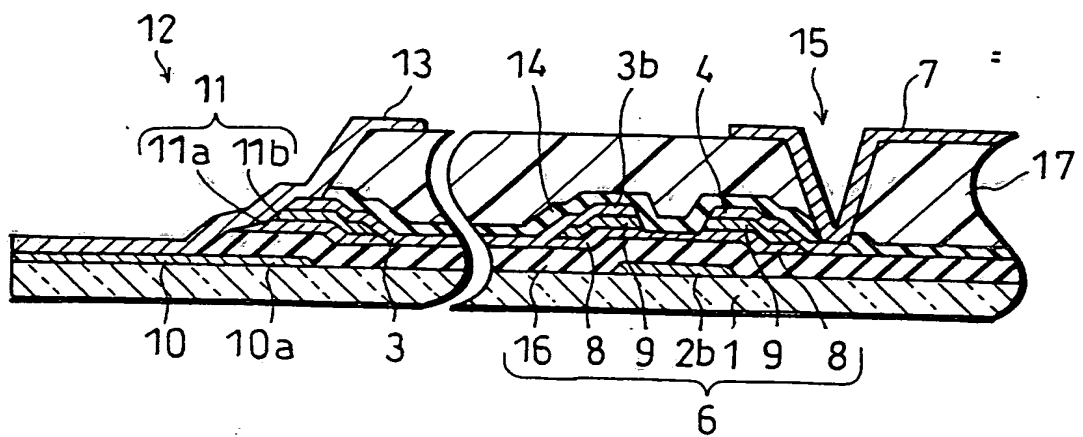


FIG. 2 (a)

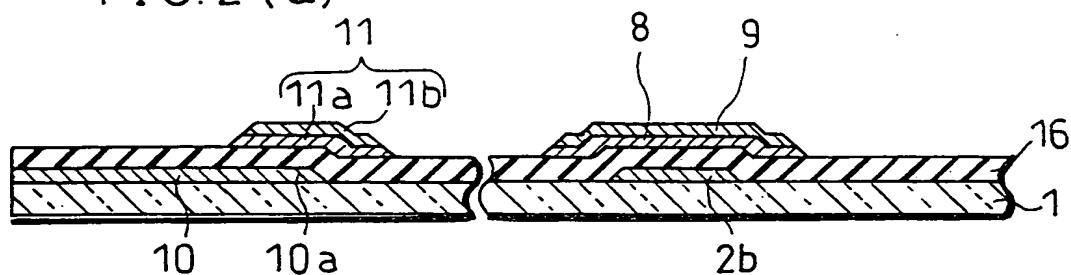


FIG. 2 (b)

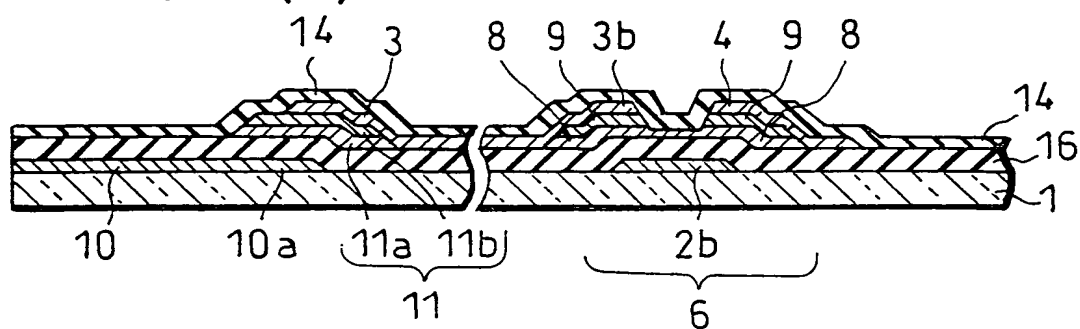


FIG. 2 (c)

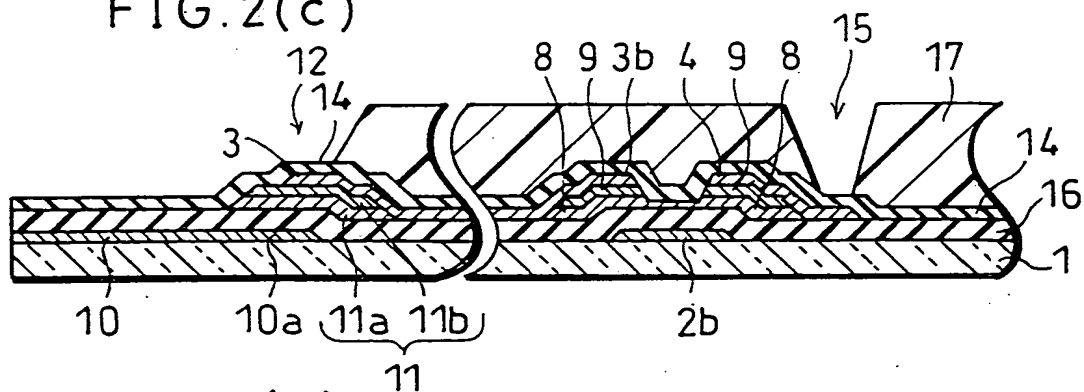


FIG. 2 (d)

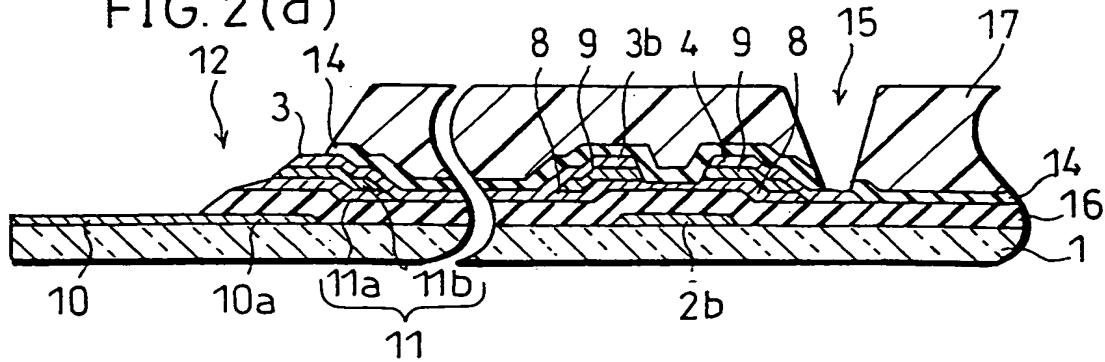


FIG. 3

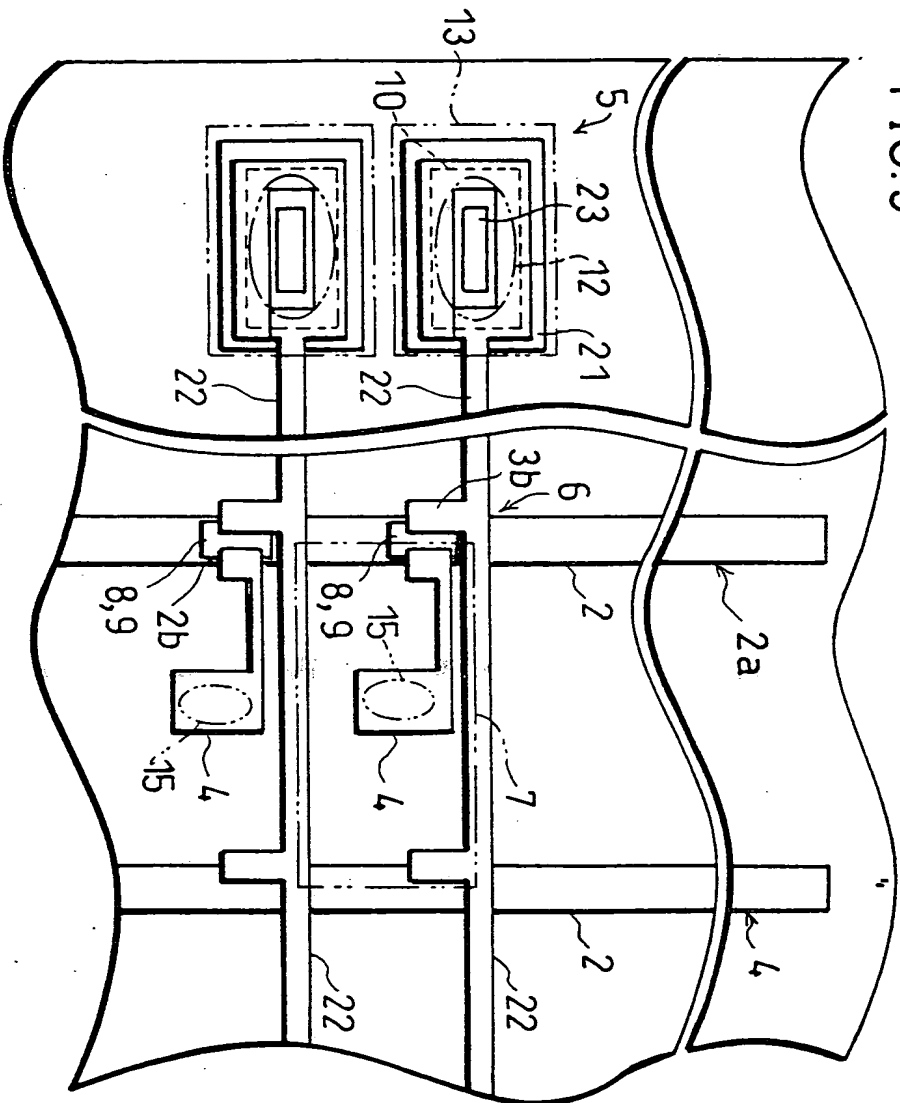


FIG. 4

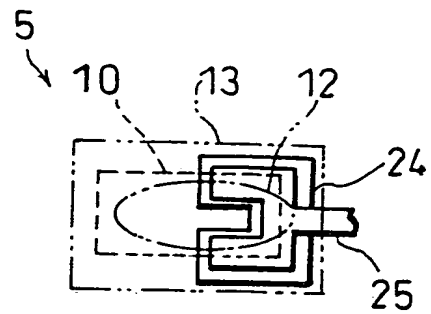


FIG. 5(a)

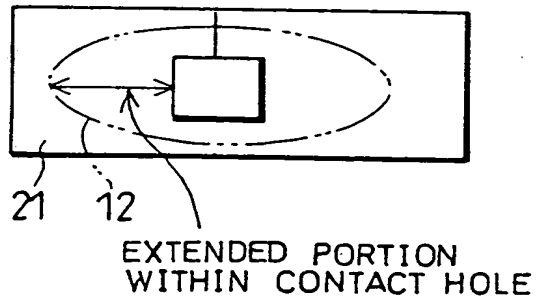


FIG. 5(b)

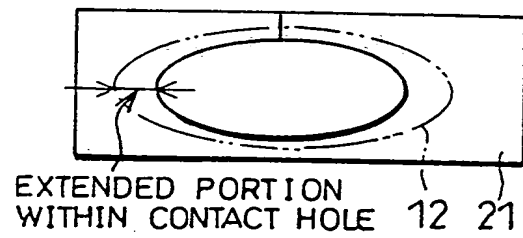


FIG. 6 (a)

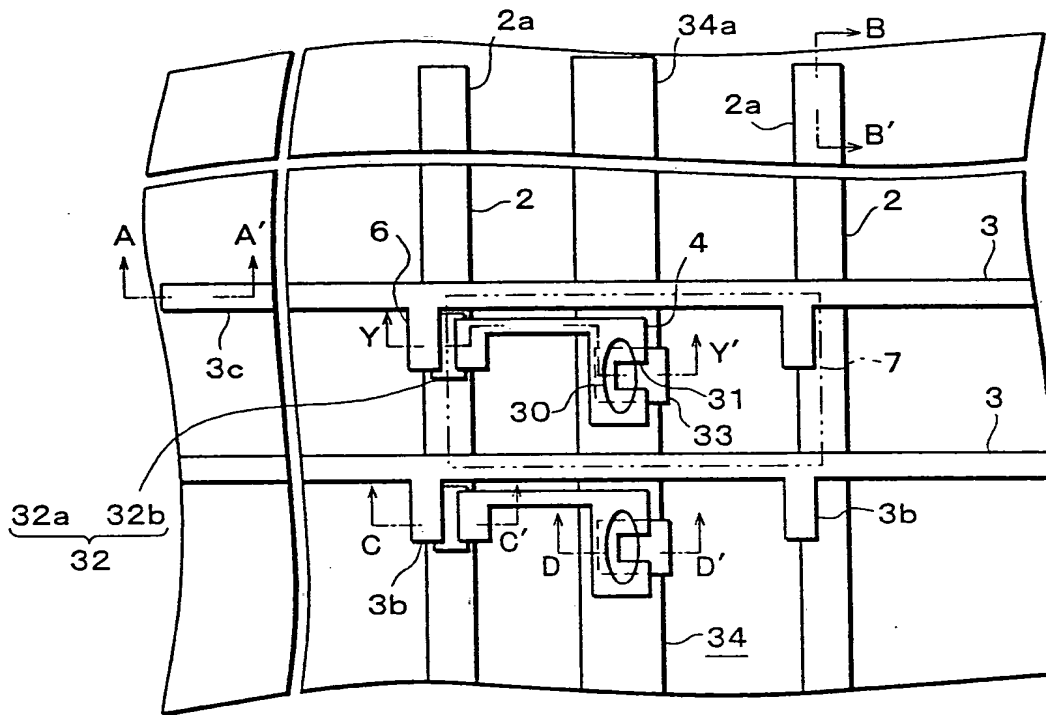


FIG. 6 (b)

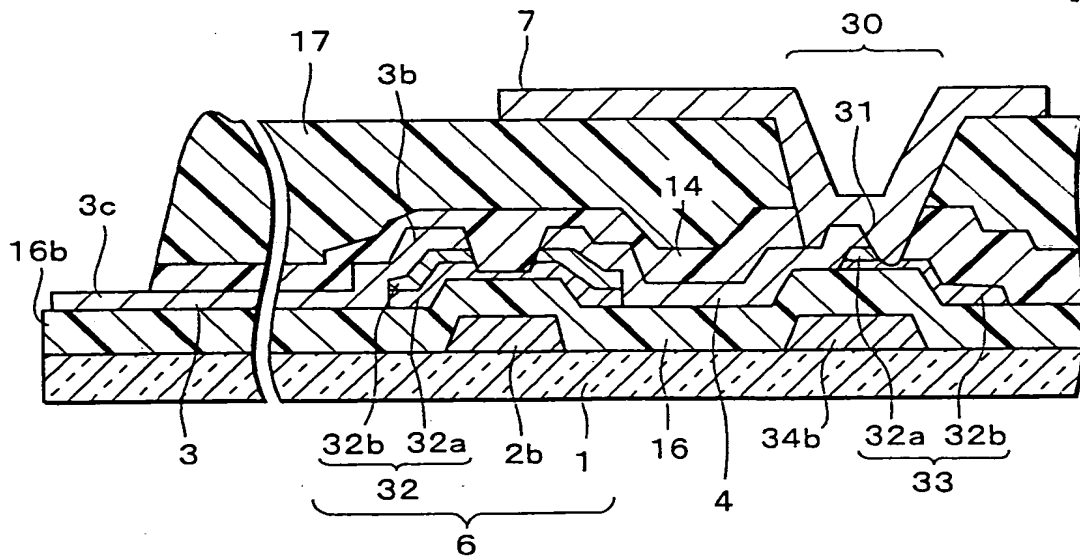


FIG. 7 (a)

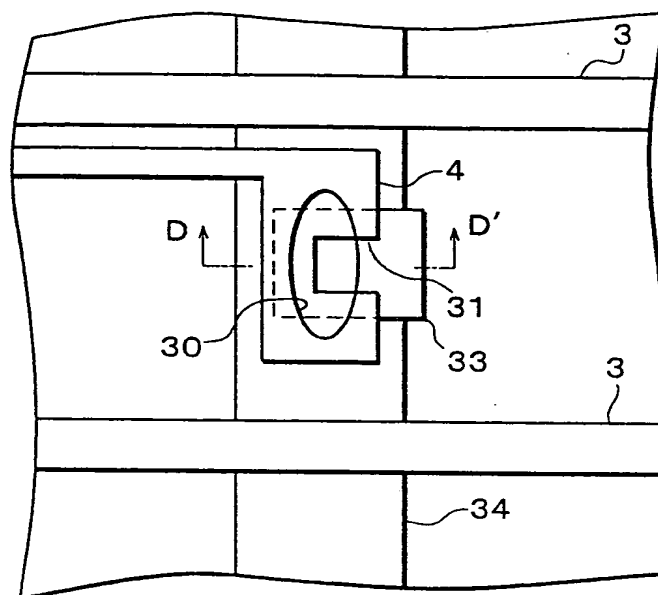


FIG. 7 (b)

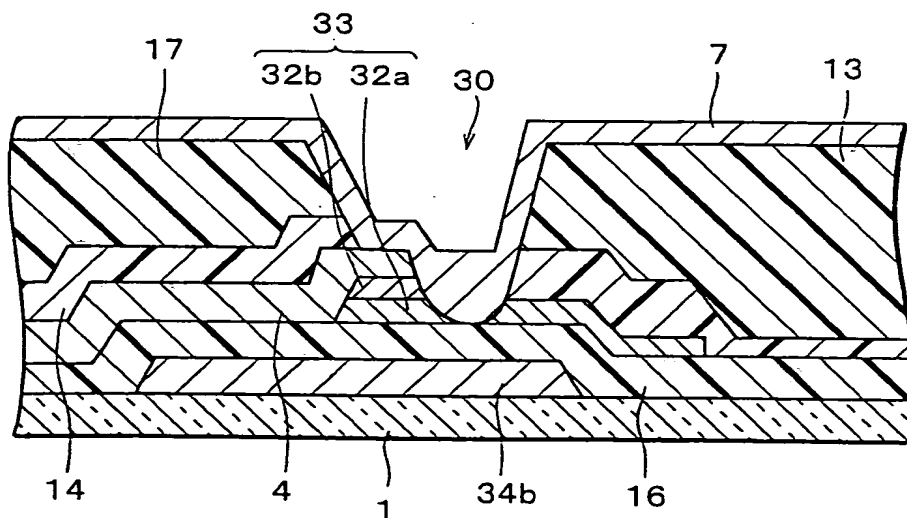


FIG. 8 (a)

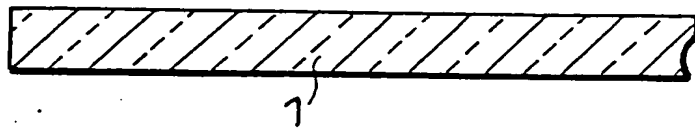


FIG. 8(b)

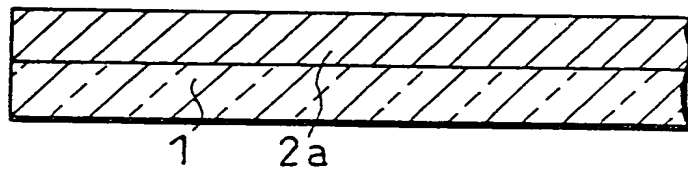


FIG. 8(c)

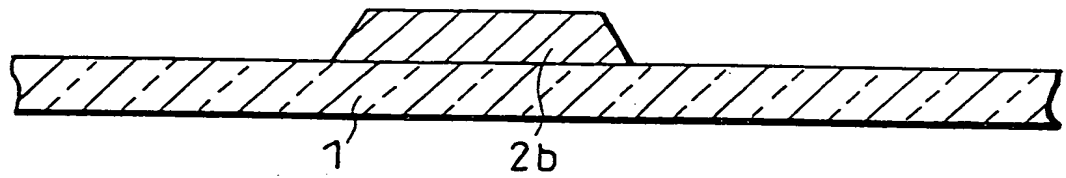


FIG. 8(d)

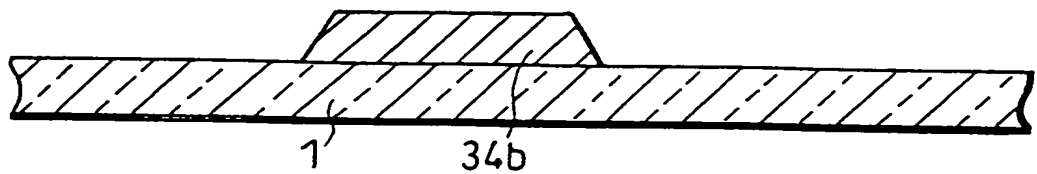


FIG.9(a)

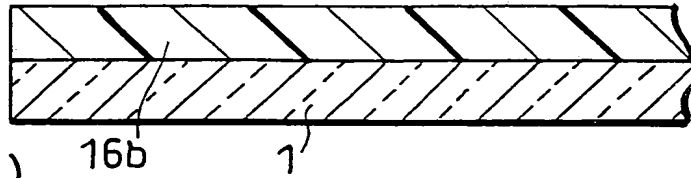


FIG.9(b)

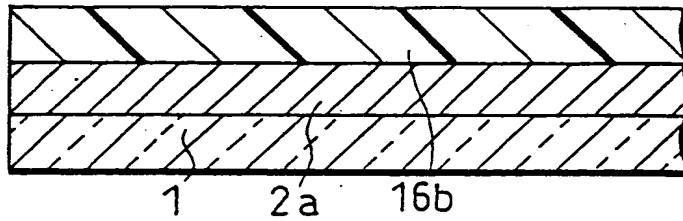


FIG.9(c)

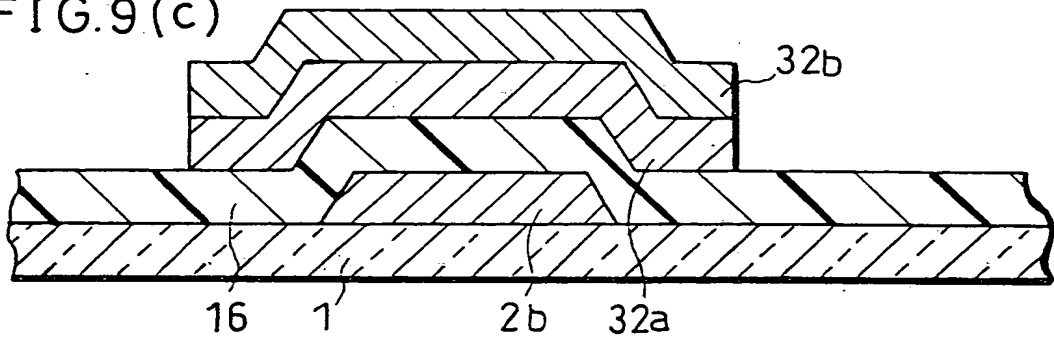


FIG.9(d)

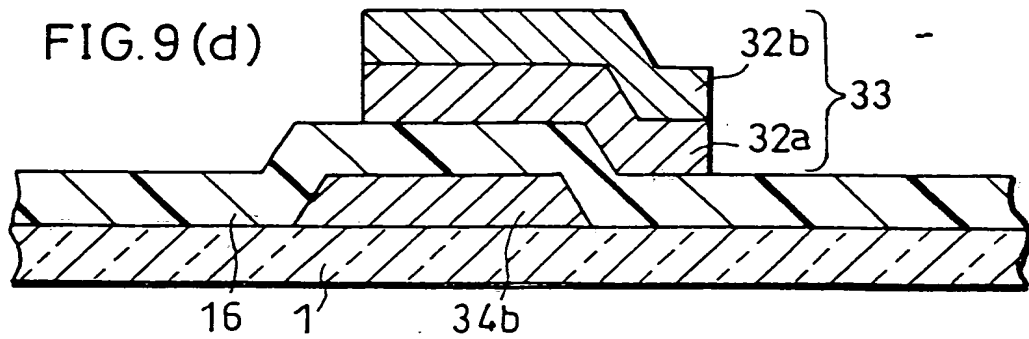


FIG.10(a)

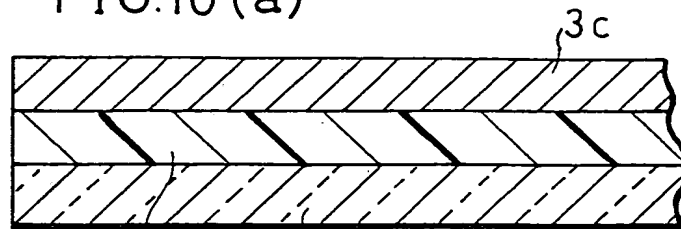


FIG.10(b)^{7b}

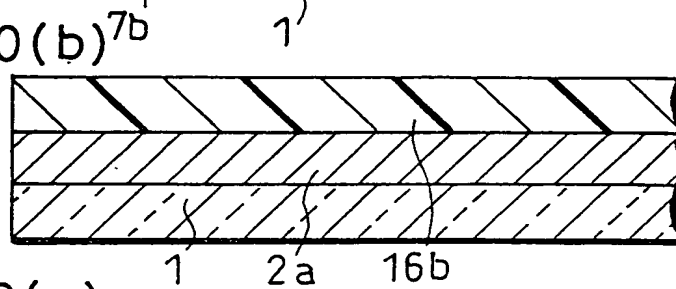


FIG.10(c)

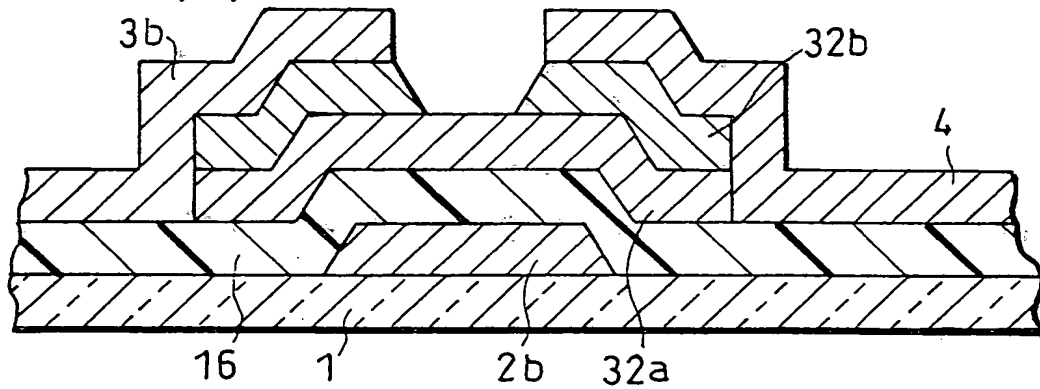


FIG.10(d)

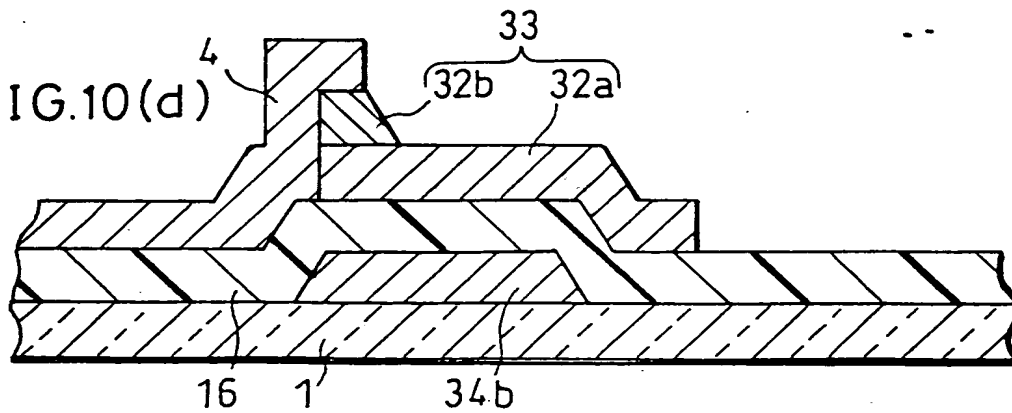


FIG. 11 (a)

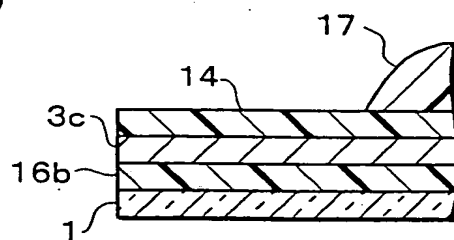


FIG. 11 (b)

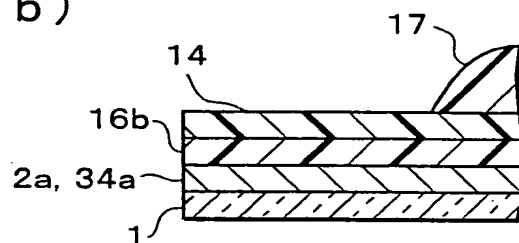


FIG. 11 (c)

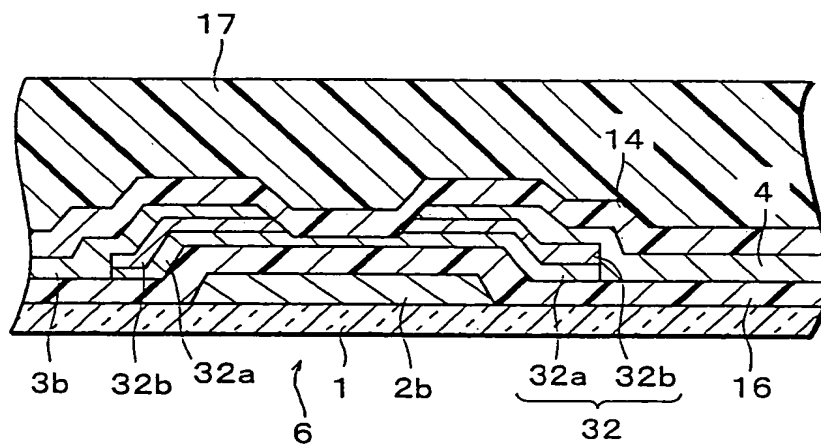


FIG. 11 (d)

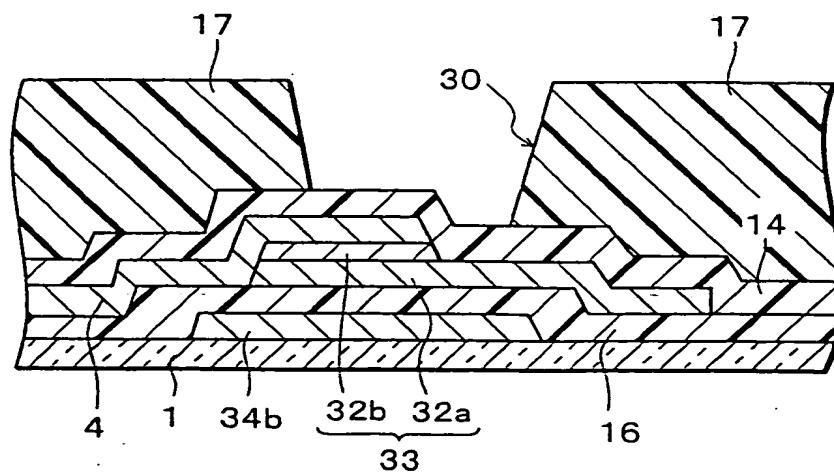
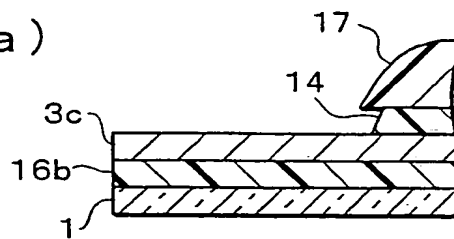


FIG. 12 (a)



F I G. 1 2 (b)

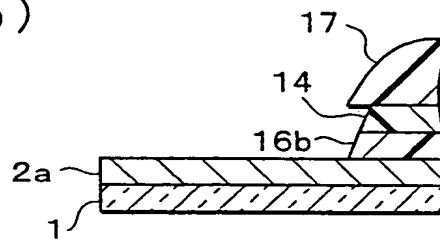


FIG. 12 (c)

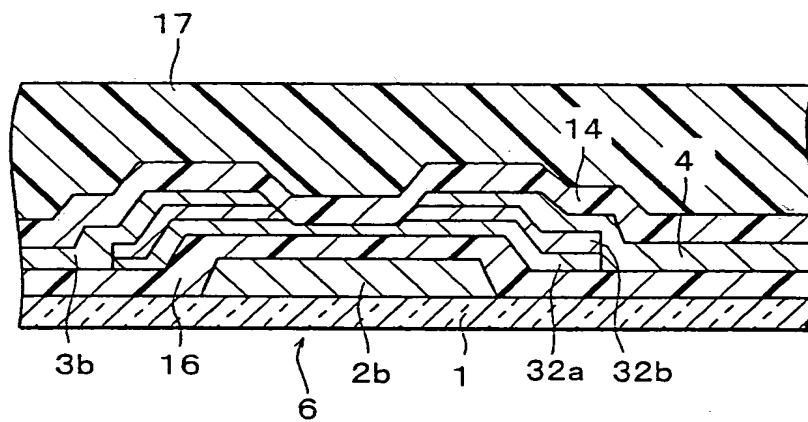


FIG. 12 (d)

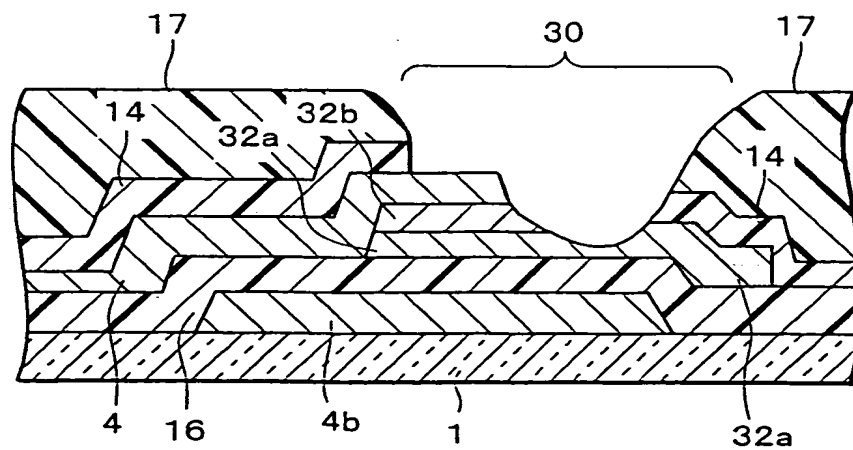


FIG. 13 (a)

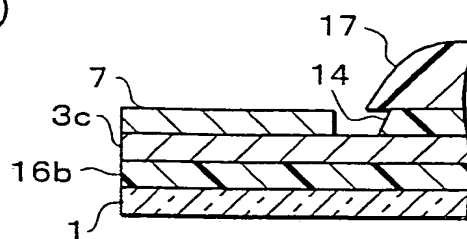


FIG. 13 (b)

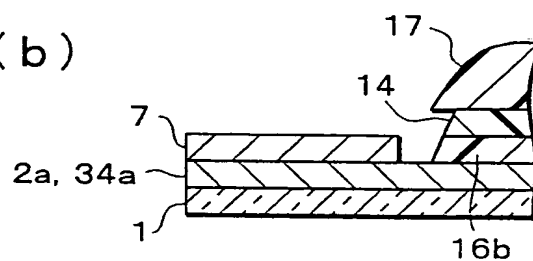


FIG. 13 (c)

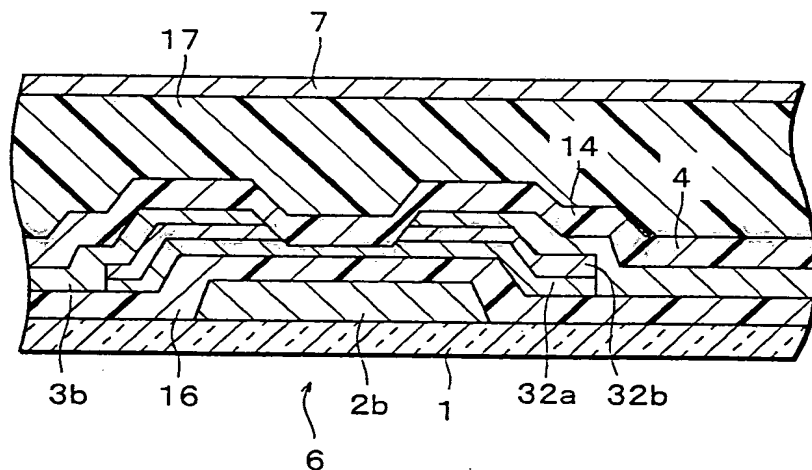


FIG. 13 (d)

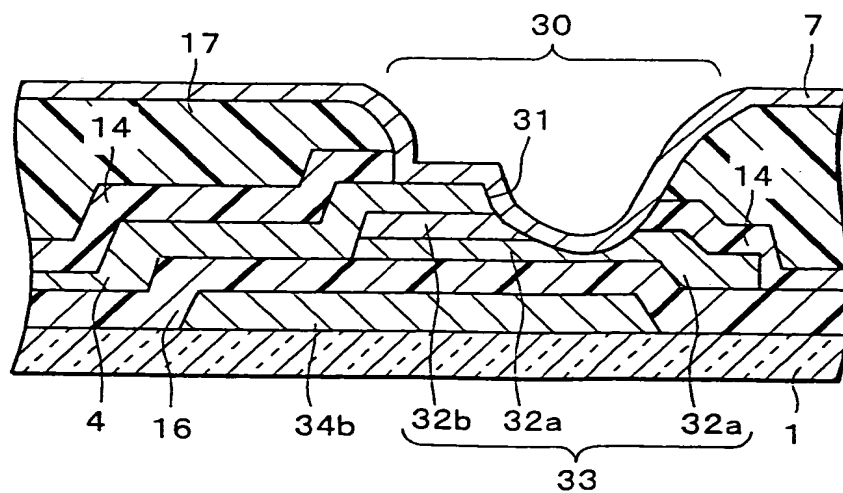


FIG. 14
(PRIOR ART)

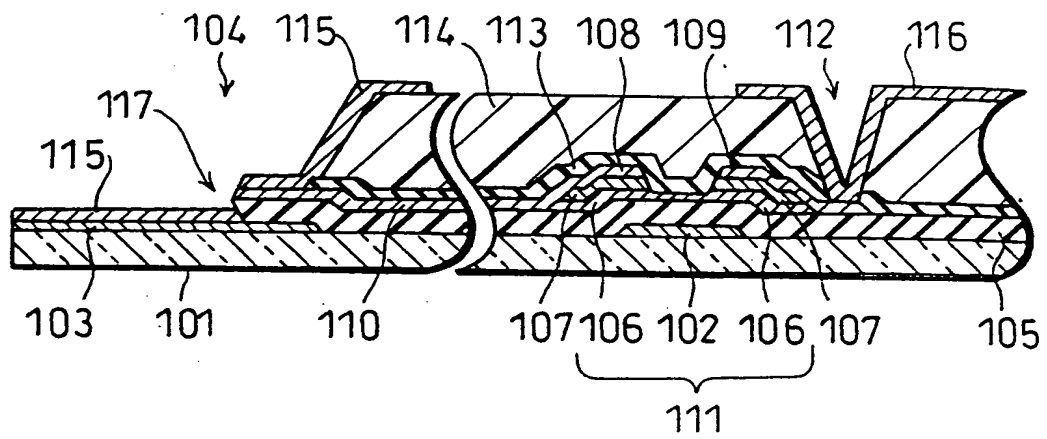


Fig. 10 is a cross-sectional view of a semiconductor device. It shows a substrate 201 with a base layer 207. A series of layers and structures are built on top, including a layer 209, a layer 209c, and a layer 209b. A central region 210 is defined by a bracket 211, which includes sub-regions 208a and 208b. Other labeled regions include 212, 213, 214, 215, 217, and 204b. The diagram uses various hatching patterns to distinguish different materials or layers.